AMENDMENTS TO THE CLAIMS:

Please revise the claims, as follows:

1. (Currently Amended) A method of forming a semiconductor substrate, said method comprising:

forming a metal back-gate over a first substrate;

forming a passivation layer on the metal back-gate to prevent the metal back-gate from reacting with radical species; ~~and~~

providing an intermediate gluing layer on said passivation layer to enhance adhesion between said metal back-gate and a handle ~~substrate;~~ substrate;

~~wherein~~ depositing a low temperature oxide (LTO) layer ~~is deposited~~ on said ~~metal back-gate~~ intermediate gluing layer; and

bonding said handle substrate to said LTO layer.

2. (Previously amended) The method of claim 1, wherein said intermediate gluing layer comprises one of a-Si, Si_3N_4 and a combined layer of a-Si and Si_3N_4.

3. (Original) The method of claim 1, wherein said forming of said metal back-gate includes depositing W, and

said forming of said passivation layer is performed after said W deposition, said passivation layer being a thin W passivation layer.

4. (Previously amended) The method of claim 3, wherein said depositing of said W comprises a physical vapor deposition (PVC) of W.

5. (Original) The method of claim 3, wherein said depositing of said W comprises a chemical vapor deposition (CVD) of W.

6. (Currently Amended) A method of forming a semiconductor substrate, said method comprising:

forming a metal back-gate;

forming a passivation layer on the metal back-gate to prevent the metal back-gate from reacting with radical species; and

providing an intermediate gluing layer on said passivation layer to enhance adhesion between said metal back-gate and a handle substrate,

wherein said forming of said ~~metal back-gate~~ passivation layer comprises:

conducting UHV desorption of native oxide on W under a pressure of 10^{-9} torr at 750°C for 5 minutes;

forming a monolayer of W-Si silicide at 625°C for 1.5 minutes using SiH_4 such that a bare W surface reacts with Si to form a monolayer of W-Si; and

performing nitridation of W-Si at 750°C for 30 minutes with NH_3 and reacting active NH_2 with W-Si to form W-Si-N.

7. (Original) The method of claim 1, wherein said metal back-gate is formed of a metal having a high melting temperature to withstand thermal treatment during semiconductor processing.

8. (Original) The method of claim 7, wherein said metal back-gate comprises one of tungsten and titanium nitride.

9. (Original) The method of claim 1, wherein said first substrate comprises a silicon-on-insulator substrate having a gate oxide formed thereon.

10. (Original) The method of claim 9, wherein said metal back-gate comprises a tungsten layer, said tungsten layer being deposited on the gate oxide.

11. (Currently Amended) The method of claim 1, wherein the metal back-gate comprises a W layer~~, and wherein said low temperature oxide (LTO) is deposited on the W layer~~.

12. (Currently amended) The method of claim 1, wherein a multilayer stack is formed on said first substrate, wherein said first substrate with said multilayer stack is bonded to a silicon handle substrate and annealed to strengthen ~~the~~ a bond across the bonding interface.

13. (Currently amended) The method of claim 11, wherein said W layer is passivated before the LTO deposition to prevent the reaction of tungsten with oxygen and the delamination at ~~the~~ a W-SiO_2 interface.

14. (Currently amended) The method of claim 1, further comprising:

annealing said metal back-gate and said handle substrate.

15. (Original) The method of claim 14, wherein said annealing occurs at temperatures below 1100 °C.

16. (Previously presented) The method of claim 15, wherein annealing conditions including any of a ramp-up rate, a ramp-down rate, a stabilization temperature, and a stabilization temperature time are optimized to minimize stress induced by thermal mismatch of different materials of said metal back-gate, said substrate, said passivation layer and said intermediate gluing layer.

17. (Previously presented) The method of claim 1, wherein said intermediate gluing layer comprises a Si-based intermediate layer.

18. (Currently Amended) A method of forming a semiconductor substrate, said method comprising:

forming a metal back-gate; and

providing a passivation layer/intermediate gluing layer between a substrate and said metal back-gate to enhance adhesion therebetween,

wherein a low temperature oxide (LTO) is deposited on said ~~metal back-gate~~ intermediate gluing layer.

19. (Currently Amended) A method of forming a semiconductor substrate, said method comprising:

growing a gate oxide on a silicon-on-insulator (SOI) ~~material~~ substrate;

depositing a refractory metal onto said gate oxide; and

forming a passivation layer, having a form of metal-Si-N, on said refractory metal, by initially desorbing a native oxide thereon to be able to form said passivation layer on a bare surface of said metal.

~~wherein a low temperature oxide (LTO) is deposited on the refractory metal.~~

20. (Original) The method of claim 19, further comprising:

depositing an insulator on said metal to form a multi-layer stack;

bonding said multi-layer stack to a second substrate, to form a bonded structure; and

annealing said bonded structure.

21. (Original) The method according to claim 19, wherein said insulator comprises one of a low temperature oxide, SiN and AlOx.

22- 38. (Canceled)

39. (Currently Amended) A method of forming a semiconductor substrate, said method comprising:

forming a metal back-gate;

forming a passivation layer on the metal back-gate to prevent the metal back-gate from reacting with radical species; and

providing an intermediate gluing layer on said passivation layer to enhance adhesion between said metal back-gate and a substrate,

wherein said providing said intermediate gluing layer on said passivation layer comprises growing said intermediate layer by in-situ ~~ultra high vacuum chemical vapor deposition (UHV-CVD)~~ growth of ~~metal-Si-N~~ a layer comprising one of a-Si, Si_3N_4, and a combination of a-Si and Si_3N_4.

40. (Previously presented) The method of claim 39, wherein said metal comprises tungsten.

41. (Currently Amended) A method of forming a semiconductor substrate, said method comprising:

forming a metal back-gate; and

providing a passivation layer between a substrate and said metal back-gate to enhance adhesion therebetween,

wherein said providing said passivation layer comprises desorbing a native oxide of said metal and growing said passivation layer by in-situ ultra high vacuum chemical vapor deposition (UHV CVD) growth of metal- Si-N.

42. (Previously presented) The method of claim 41, wherein said metal comprises tungsten.

43. (Currently Amended) A method of forming a semiconductor substrate, said method comprising:

growing a gate oxide on a silicon-on-insulator (SOI) material;

depositing a refractory metal onto said gate oxide; and

forming a passivation layer on said refractory metal,

wherein said forming said passivation layer comprises desorbing a native oxide of said metal and growing said passivation layer by in-situ ultra high vacuum chemical vapor deposition (UHV CVD) growth of metal-Si-N.

44. (Previously presented) The method of claim 43, wherein said metal comprises tungsten.

45. (Currently amended) A method of forming a semiconductor substrate, said method comprising:

forming a metal back-gate; and

providing a passivation layer between a substrate and said metal back-gate to enhance adhesion therebetween,

wherein said passivation layer is grown by first desorbing a native oxide of said metal and then growing an in-situ layer such that subsequent oxidation of a metal is substantially prevented.

46. (Currently amended) The method of claim 45, wherein said in-situ growth of said passivation layer comprises a chemical vapor deposition (CVD) growth of metal -Si-N.

47. (Previously presented) The method of claim 46, wherein said chemical vapor deposition comprises an ultra high vacuum (UHV) deposition.